ME EX 3 cm - II (CBCG3) SWb-DDRA 20/11/2017

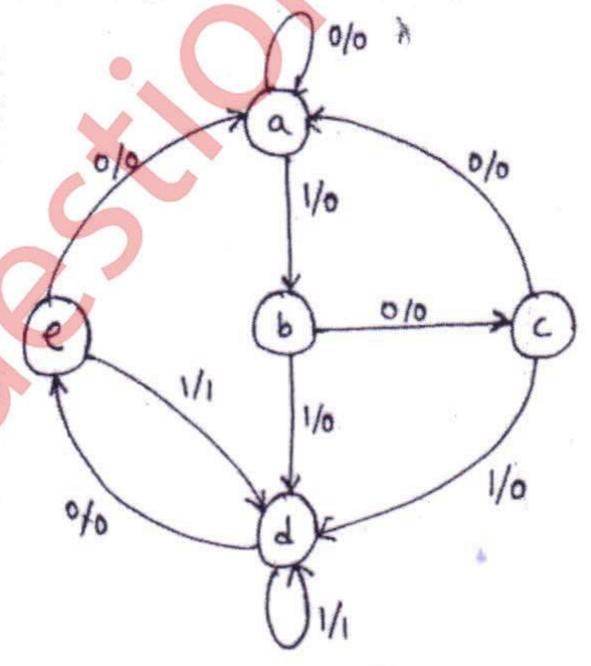
Q.P. Code: 24426

(3 Hours)

[Total Marks: 80]

## N.B.: (1) Question No. 1 is Compulsory.

- (2) Attempt any three questions out of remaining five.
- (3) Each question carries 20 marks and sub-question carry equal marks.
- (4) Assume suitable data if required.
- 1. (a) Write the differences between signal and variable. (5)
  - (b) Explain the concept of Bad clocking and Good clocking. (5)
  - (c) Draw a state diagram for overlapping sequence detector for the serial (5) sequence "11011". Use Mealy model.
  - (d) Explain various data types in VHDL. (5)
- 2. (a) Write a VHDL code for 4 bit carry look ahead adder. (10)
  - (b) Using the Data / controller partition method, draw ASM charts for shift and ADD multiplier and explain it in detail. (10)
- 3. (a) Using WITH / SELECT / WHEN write a VHDL code for 16:1 (10) multiplexer.
  - (b) Draw state diagram for BCD counter and write a VHDL code for it. (10)
- 4. (a) Identify the redundant states, if any for the following state diagram (10) (shown in Figure 1) of a sequential machine and design it using JK flipflops.



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Figure 1.

- (b) Explain operation of 4 bit parallel multiplier with neat diagram. (10)
- 5. Write short notes on any three of the following: (20)
  - (a) Divider using VHDL.
  - (b) RTL simulator.
  - (c) Clock management in FPGA.
  - (d) Odd parity checker for serial data,
- Design a Traffic Light Controller (TLC) having operational characteristics summarized in the following table. Use VHDL code. (This is simple TLC table which shows R or G or Y in two directions only. State RG means in one direction Red signal and other direction Green signal).

| State | Operation Mode |           |                                       |
|-------|----------------|-----------|---------------------------------------|
|       | Regular Time   | Test Time | Stand by Time                         |
| RG    | 60 sec         | 1 sec     |                                       |
| RY    | 05 sec         | 1 sec     | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 |
| GR    | 50 sec         | l sec     | 3 2 6 2                               |
| YR    | 05 sec         | 1 sec     |                                       |
| YY    |                |           | Indefinite                            |

Assume that a 50 Hz clock is available. The TLC has following 3 modes of operation.

- (i) Regular mode: Four states each with an independent time as shown in table, passed to the circuit by means of a constant.
- (ii) Test mode: In this, all preprogrammed times are overwritten with 1 sec.
- (iii) Standby mode: In this, in both directions yellow lights will be activated.