FE | Sem-II | NEP-2020 | All Braches | DE | SH-2025 |

(03 HOURS) (MAX. MARKS : 60)

5/12/2025

QP-10097070

Note:

1. Question **No. 1** is compulsory.
2. Attempt **any three** questions out of remaining **five** questions.
3. Assume suitable data wherever necessary.
4. Figures to right indicate full marks.

			Marks
Q.1		Answer the following **(Any Five)**	
	a.	State and Prove DE Morgan's theorem	**03**
	b.	Realize AND Gate Using NOR Gate Only	**03**
	c.	Design Full Subtractor using only NAND gates	**03**
	d	Compare Moore with mealy circuits	**03**
	e	Design full adder using 8:1 MUX.	**03**
	f	What is F/F? Give its types	**03**
Q.2	**a.**	What is PLD? Explain in detail and Give its advantages.	**08**
	b.	Design and implement 2-bit Magnitude Comparator.	**07**
Q.3	**a.**	Explain the operation of an SR Flip Flop using excitation table. Give its Truth Table and Characteristic Equation	**08**
	b.	Simplify the Boolean expression using K-map and implement using Logic gates $F(ABCD)=\Sigma\, m(1,2,3,5,6,7,10,11) + d(9,12,15)$	**07**
Q.4	**a.**	Explain 3-bit asynchronous up- Down counter.	**08**
	b.	Explain working of Decoder. Design full adder using 3 :8 Decoder	**07**
Q.5	**a.**	If $f(A,B,C)=\sum m(0,3,5,7)$, write its truth table and express given function in SOP and POS form.	**08**
	b.	Implement the Boolean function using8: 1 multiplexer $f(A, B, C, D) = \Sigma m(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$	**07**
Q.6		Write short note on a. State reduction Techniques b. PLA c. Twisted Ring Counter	**05**

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