Paper / Subject Code: 42573 / Mixed Signal VLSI Design (DLOC - III)

1T01137 - B.E.(Electronics Engineering)(SEM-VII)(Choice Base Credit Grading System) (R-19-20) (C Scheme) / 42573 - Mixed Signal VLSI

Design (DLOC - III)

QP CODE: 10016269 DATE: 14/12/2022

(3 Hours) Total Marks: 80

N.B: (1) Question No.1 is compulsory and solves ant three questions from remaining questions.

- (2) Assume suitable data if necessary.
- (3) Draw neat and clean figures.

1. **Answer any four:**

- (a) Explain trade off in Analog design with the help of analog design octagon 5
- (b) For N channel MOSFET draw i) small signal model ii)small signal model with 5 channel length modulation iii)small signal model with body effect?
- (c) Explain importance of Miller theorem 5
- (d)Explain noise in differential amplifier circuit?
- (e) Draw and explain 3-bit flash ADC with its methodology of conversion?
- 2. (a) Derive voltage gain of diode connected load CS amplifer?
 - (b) Derive equation of differential gain, common mode gain, CMRR of differential **10** amplifier?
- 3. (a)Explain in detail how to generate temperature independent reference? 10
 - (b) Explain correlated and uncorrelated noise sources in CMOS circuit?
- 4 (a) Design an amplifier that meet the following specification with a phase margin of 60.assume the channel length is to be $1\mu m$ Av>5000v/v, Vdd=2.5, Vss=-2.5v, GB=5MHz, CL=10pf,

Av>5000v/v, vdd=2.5, vss=-2.5v, GB=5MHz, CL=10pi,

SR>10v/µsec, Vout range=+/- 2V, ICMR= -1 to 2V, Pdiss≤ 2mw.

- 5 (a)Explain Mixed signal layout issues in detail? 10
 - (b)Explain noise in single stage CS amplifier circuit?

QP CODE: 10016269

6 Write short notes(any three)

20

- (a) White and flicker noise in MOSFET
- (b) Cyclic DAC
- (d) Noise bandwidth
- (e) Operational Amplifier Design Parameters

16269

Page 2 of 2