TE-(ELEX) - sem VI - R-19 - C-Scheme 14.05.25

Time: 3 Hours Total Marks: 80

Note:
1) Question No 1 is Compulsory.
2) Answer any three from the remaining questions.
3) Assume suitable data wherever required

Q1. Solve any four of the following (20)

a. Explain Oxide related capacitances in MOSFET.

b. Write short on High-speed adders.

c. Implement the function F= $\overline{A+(B+C).(D+E)}$ using standard CMOS Logic

d. Implement 4X4 NAND based ROM array.

e. Write short Notes on 4 X 4 Barrel Shifter.

Q2.a Compare the full scaling and constant voltage scaling models of MOSFET. Demonstrate the effects of scaling on the area, delay, power consumption and current density of the device. (10)

b. Explain CMOS inverter characteristics mentioning all regions of operation. (10)

Q3.a Distinguish with application area Pass transistor logic, NMOS logic and CMOS logic. (10)

b. Draw 6T SRAM cell and explain its read write and refresh operation. (10)

Q4.a Compare Static CMOS and Pseudo NMOS design styles. Implement 2 input NAND gate using pseudo NMOS design style. (10)

b. Draw and explain LATCH UP in CMOS. (10)

Q5.a Draw Carry Look Ahead Adder chain using Dynamic CMOS Logic. (10)

b. Explain 4:1 Multiplexer using NMOS pass transistor. Explain the advantages of using Transmission gates. (10)

Q6. Explain any four (20)

a. BJT and MOS Technologies.

b. D flip flop using CMOS logic.

c. Sense Amplifier.

d. Power dissipation in CMOS.

e. ZIPPER logic design style.

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