N. B.	Time: 5 ms.	
	compulsory.	
	er any three out of the remaining five questions.	
	es to the right indicate marks.	
4. Answe	er to the questions should be grouped and written together.	
0.1		5
Q1.	Solve any four out of five	5
a.	What is the Over Drive Voltage and its Significance.	_
b.	Explain ADC Specifications.	5 5
c. d.	Compare common source, Common gate and common Drain Amplifier in brief. What is the drawback in Current Mirror circuit? How to overcome it?	5
e.	Explain various issues associated with Mixed Signal Circuit Layout.	
Q2 a.	Draw and explain the Input common mode response of differential amplifier.	10
b.	For a NMOS Amplifier with driver (M1) with Vin as the input voltage and PMOS as a load (M2) with Vb as the input gate Voltage to the PMOS. The $V_{DD} = 1.8V$. $\lambda_1 = 0.1 \ V^{-1}$, $\lambda_2 = 0.15 \ V^{-1}$, $u_n Cox = 200 uA/V^2$, $ Vth = 0.4V$	10
	The Amplifier should provide gain of 10 with bias current of 0.5mA.	
	Compute (W/L) of M1.	
Q3	Draw and explain the Pipeline DAC.	10
b	Derive the Voltage Gain for CS Stage with Diode Connected Load.	10
04		20
ER OV	Design a two stage Op-Amp for the following specifications Design a two stage Op-Amp with a phase margin of 60 degree and channel Length	
	=1um $Av > 3500v/v$, $Vdd = 2.5v$, $Vss=-2.5v$, $Gain Bandwidth = 6MHz$	
	Cload= 10pf , SR. 10 V/us , Vout range = $+2\text{ to }-2\text{ v}$,	
	ICMR = -1.125 V to $+2$ V , Power Dissipation < 2 mw	
2/6/	$\epsilon_0 = 8.854 \times 10^{-14} \text{ F/cm}$	
	$\varepsilon_{\rm Si} = 11.7 \ \varepsilon_{\rm O} \ \rm F/cm$	
	$\varepsilon_{\text{OX}} = 3.9 \ \varepsilon_{\text{O}} \ \text{F/cm}$ Threshold Voltage (NMOS) = 0.7V Threshold Voltage (PMOS) = -0.7V	
50,1	Channel length modulation index (NMOS) = 0.04 V^{-1} Channel length modulation index (PMOS) = 0.05 V^{-1}	
Q5 a b.		10 10
S Q6	Write short notes on	
a.		5
b.	Noise in MOSFETs.	5
c.	CMOS band gap reference generator.	5
d.	Triple CASCODE circuit	5