Time: 3 hours **Max. Marks: 80**

N.B. : (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

Q1 Solve any Four **5 marks each**

A Explain the V-I characteristics of a p-n junction diode under forward and reverse bias conditions. State the diode current equation and define each term.

B A zener diode has a breakdown voltage of 5.6 V and a maximum power dissipation of 500 mW. Calculate the maximum allowable current through the diode. Also, explain its operation as a voltage regulator with a neat circuit diagram.

C Explain the concept of the DC load line and how the Q-point is located on it for a CE configuration. Why is the choice of Q-point critical?

D Describe the roles of coupling capacitors, bypass capacitors, and parasitic capacitors in shaping the frequency response of an amplifier.

E Explain the concept of Crossover distortion in a Class B power amplifier

Q2 10 Marks each

A With a neat circuit diagram, explain the working of a two-transistor E-MOSFET differential amplifier. Derive expressions for: (i) differential-mode gain (A_D), (ii) common-mode gain (A_C), and (iii) CMRR. Explain the significance of the constant current source in the tail and how it improves CMRR.

B Explain the working of a two transistor constant current source with the help of neat circuit diagram and derive the output current equation.

Q3 10 marks each

A Explain the effect of source resistance and load resistance on the voltage gain and bandwidth of an amplifier?

B Draw a small signal equivalent circuit of an E-MOSFET CS amplifier given in fig.(2) and derive the expression for voltage gain, input resistance and output resistance.

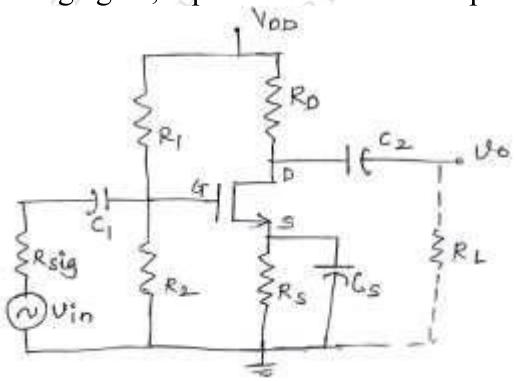


Fig.(2)

X525YF1AB1FX525YF1AB1FX525YF1AB1FX525YF1AB1F

Q4 10 marks each

A With a neat circuit diagram, explain the voltage-divider bias configuration for a BJT amplifier. Derive the expressions for the base current (I_B), collector current (I_C), and the Q-point (V_{CE}). Use Exact Analysis.

B Compare BJT, JFET, and E-MOSFET with respect to construction, control mechanism, input impedance, and typical applications.

Q5 10 Marks each

A Calculate low cutoff frequencies due to coupling and bypass capacitors of the circuit given in fig. 5

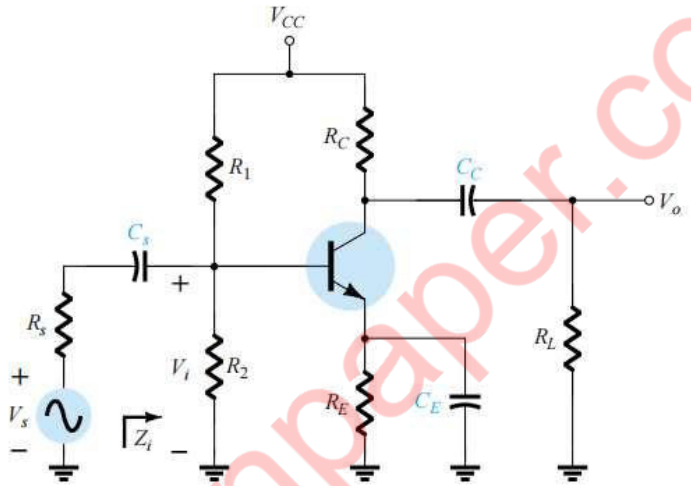


Fig.(5)

$R_s = 1\ \text{k}\Omega,\ R_1 = 40\ \text{k}\Omega,\ R_2 = 10\ \text{k}\Omega,\ R_E = 2\ \text{k}\Omega,\ R_C = 4\ \text{k}\Omega,\ R_L = 2.2\ \text{k}\Omega$

$C_s = 10\ \mu\text{F},\ C_C = 1\ \mu\text{F},\ C_E = 20\ \mu\text{F}$

$\beta = 100,\ r_o = \infty\ \Omega,\ V_{CC} = 20\ \text{V}$

B For a Class B amplifier providing a 20 V peak signal to a 16 Ω load (speaker) and a power supply of V_{CC} = 30 V, determine the input power, output power and circuit efficiency.

Q6 10 Marks each

A Draw and explain a series fed class A power amplifier with the help of neat diagram and waveforms and derive the expression of power efficiency

B A CE BJT amplifier has the following parameters: β = 120, r_π = 1.2 kΩ, r_O = 40 kΩ, gm = 100 mA/V, R_C = 3.3 kΩ, R_L = 10 kΩ, R_E = 600 Ω, R_B = 22 kΩ. Using the small signal hybrid-π model: (i) Calculate the voltage gain $A_V = V_O/V_i$. (ii) Find the input impedance Z_i (iii) Find the output impedance Z_O.

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