09-06-2026 SE EXTC SEM-III C SCHEME DSD QP CODE: 20011953

Duration: 3 Hours **[Max Marks: 80]**

NB:
1. **Question no. 1 is compulsory.**
2. **Out of remaining questions, attempt any 3 questions.**
3. **All questions carry equal marks.**
4. **Assume suitable data, if required and state it clearly.**

Q1. Attempt the following. (Any four)

	a)	Perform the following operation using 2's complement method i)(28-42) 10 ii)(52-18) 10	**5**
	b)	For decimal numbers 0-15 write gray codes	**5**
	c)	Convert the given Boolean expression to minterms : Y= ABC+AC	**5**
	d)	Explain at least 5 parameters of logic families in brief	**5**
	e)	Write short notes on SRAM and DRAM	**5**
Q2	**a)**	Design 3 bit Asynchronous UP/DOWN counter and draw the logic diagram for the same.	**12**
	b)	Design a Mod-10 Synchronous Counter using T F/Fs. whether the counter is self starting?	**08**
Q3	**a)**	Minimize the following SOP using K-Map and implement using universal gates. $F=\sum m(0,2,6,7,8,9,10,13)+d(1,3,4,5,14,15)$	**10**
	b)	Obtain the minimal expression using tabular method $F=\sum m(1,2,3,5,6,7,8,9,12,13,15)$	**10**
Q4	**a)**	What are shift registers? How they are classified Explain any one type of shift register with proper logic diagram.	**10**
	b)	Explain Full adder circuit using PLA having three inputs, 8 product terms and two outputs.	**10**
Q5	**a)**	Explain the Johnson counter design for initial state 0110.From initial state explain and draw all possible states.	**10**
	b)	Explain ring counter design having initial state 01011.From initial state explain all possible states. Draw the timing diagram of the counter.	**10**
Q6	**a)**	Simplify the following expression using Boolean algebra $Y(A,B,C)=\sum m(0,1,2,3,4,5,6,7)$	**10**
	b)	Write VHDL code for half adder operation and explain.	**10**

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