18 NOV 2025 SE EXTC SEM-III C SCHEME DSD QP CODE: 10094423

Duration: 3 Hours **[Max Marks: 80]**

NB:
1. **Question no. 1 is compulsory.**
2. **Out of remaining questions, attempt any 3 questions.**
3. **All questions carry equal marks.**
4. **Assume suitable data, if required and state it clearly.**

Q1. Attempt the following. (Any four)

	a)	Explain Excess-3 code and Gray code with examples	5
	b)	Implement OR operation using Universal gates.	5
	c)	Implement a 4:1 multiplexer.	5
	d)	Differentiate between Latches and Flip-Flops.	5
	e)	Compare asynchronous and synchronous counters.	5
	f)	Give classification of PAL & PLA.	5
Q2	a)	Solve using Quine McClusky method $f(A,B,C,D) = \Sigma m\ (0,1,2,4,6,8,9,11,13,15)$	12
	b)	Implement a full adder using half adder.	08
Q3	a)	What is a binary comparator? Design 2-bit magnitude comparator and implement using logic gates.	10
	b)	Draw the block diagram of BCD adder using IC 7483 and show with example the addition of two BCD numbers.	10
Q4	a)	Design a MOD-10 (BCD) counter using flip-flops..	10
	b)	A combinational circuit is defined by the following functions. $F_1(A, B, C) = \sum m(0, 1, 3, 4)$. $F_2(A, B, C) = \sum m(1, 2, 3, 4, 5)$ Implement the circuit with PLA having 3-inputs, 4product terms and 2 outputs	10
Q5	a)	Convert i) SR flip-flop to JK flip-flop [5] ii) D flip flop to T flip flop [5]	10
	b)	What is the difference between a ring counter and a twisted ring counter? Draw and explain the 4-bit ring counter.	10
Q6	a)	Write short note on **any two:** i) Carry Look ahead Adder ii) Serial -In- Parallel -Out Shift Register iii) Characteristics of logic families iv) VHDL	10
	b)	Write a VHDL code for a 4-bit binary adder.	10

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