08 DEC 2025 SE EXTC (SEM-III) (NEP-2020) DSD QP CODE: 10099697

(2 Hours) **(Total Marks: 60)**

N.B.:
1) **Question No. 1 is compulsory.**
2) **Answer any three questions from Q.2 to Q.6.**
3) **Figures to the right indicate full marks.**
4) **Assume suitable data if required.**

Q.1		Answer any **Five** of the following.	[15]
A		State and prove De-Morgans theorem	[03]
B		Compare CMOS and TTL logic families.	[03]
C		Construct a full adder using two half adders.	[03]
D		Convert following equation into canonical form: $Y = AB + A\bar{C} + BC$	[03]
E		Construct a 16:1 multiplexer using 4:1 multiplexer.	[03]
F		Compare Mealy and Moore machine.	[03]
Q.2	A	Design Gary to Binary code converter.	[08]
	B	Explain working of 4-bit asynchronous up-down counter and draw the output waveforms.	[07]
Q.3	A	Implement F (A, B, C, D) =Σm (0,2,3,6,8,9,12,14) using 8:1 multiplexer.	[08]
	B	Design a synchronous Mod-8 up-counter using J-K Flip Flop.	[07]
Q.4	A	What is race condition in flip-flops? How it is avoided.	[05]
	B	What is shift register? Explain SISO and PIPO with example.	[05]
	C	Write a VHDL code for Full Adder.	[05]
Q.5	A	Explain any practical 3:8 decoder IC.	[05]
	B	Convert D to T flip-flop.	[05]
	C	Write a short note on FPGA and CPLD.	[05]
Q.6	A	Explain ripple carry and carry lookahead adders with block diagrams.	[08]
	B	Draw and explain the working of a 4-bit Jhonson counter with timing diagram.	[07]

****