## Paper / Subject Code: 40623 / Digital Electronics

1T00834 - S.E.(Electiral Engineering)(SEM-IV)(Choice Base Credit Grading System) (R-19) ('C' Scheme) / 40623 - Digital Electronics QP CODE: 10016485 DATE: 14/12/2022 **Duration: 3hrs** Total Marks: 80 **Note:** 1. Q. no. 1 is compulsory 2. Solve any three questions from the rest 3. Make suitable assumptions wherever applicable Q. no. 1. Answer any four (20)a. Draw the diagram of a three input AND gate and write the truth table and logic expression b. Convert  $(247)_{10}$  in to octal and Hex equivalent. c. Explain what DCTL logic family is? d. Realize a half adder logic circuit using gates. e. What is a latch? Explain. Q. No. 2. a. Perform the following subtraction using 2's complement method. (10)i. 01000-01001 ii. 01100-00011 (10)b. Write short note on characteristics of digital IC. Q.No.3 a. Explain the TTL logic with the help of TTL NAND gate realization. (10)b. Minimize the four variable logic function using K map (10) $f(A,B,C,D)=AB\bar{C}D+\bar{A}BCD+\bar{A}\bar{B}\bar{C}+\bar{A}\bar{B}\bar{D}+A\bar{C}+A\bar{B}C+\bar{B}$ Q. No. 4. a. Minimize the following logic function and realize using NAND and NOR gate (10)  $f(A,B,C)=\Sigma m(0,1,4,6,8)$ b. Design a 6 bits binary to BCD converter using multiplexer. (10)Q. No. 5 a. Write short note on J-K master slave Flip flop. (10)b. Design a three bits asynchronous binary counter using flip flop. (10)Q. No. 6 (20)Write short not on any 2 A 3 bit R-2R D/A converter ii. Dual slope A/D converter iii. Classification of memory

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Page 1 of 1