Time: 3 Hours **Marks: 100**

N.B. : (1) **All** questions are **compulsory**.
(2) **Figures** to the **right** indicate **full** marks.
(3) Draw **neat** diagrams wherever **necessary**.
(4) Symbols have usual meaning unless otherwise stated.
(5) Use of **non-programmable** calculator is allowed.

Q1. Attempt any **two:---**

(i) Explain JFET as multiplexer and voltage controlled resistor. **10**

(ii) Sketch the cross section of Depletion MOSFET and Enhancement MOSFET. Explain the use of MOSFET to drive passive and active load. **10**

(iii) Explain the use of SCR as half wave rectifier and derive the expression for its average output voltage and current. **10**

Q2 Attempt any **two:---**

(i) Draw a neat circuit diagram of the basic configuration of instrumentation amplifier using three operational amplifiers. Explain its working and derive an expression for its voltage gain. **10**

(ii) With the help of a neat circuit diagram, explain the working of triangular wave generator using Schmitt trigger and integrator. Sketch the waveforms at output terminals of Schmitt trigger and integrator. What is the expression for frequency and peak to peak voltage of the triangular wave? **10**

(iii) What is Differential Amplifier? Explain with neat circuit diagram the working of an emitter coupled differential amplifier with single ended input and double ended output. **10**

Q3 Attempt any **two:---**

(i) Draw a neat circuit diagram of a transistorized astable multivibrator. With the help of necessary waveforms explain its working and derive an expression for frequency of output wave. **10**

(ii) Draw the circuit diagram of IC 555 to work as monostable multivibrator. Explain its operation and sketch the relevant waveforms. Obtain expression for the output pulse width. **10**

(iii) With the help neat circuit diagram, explain the working of series voltage feedback regulator. Derive an expression for its output voltage and power dissipation. **10**

Q4 Attempt any **two:---**

(i) Explain the working of two inputs CMOS NAND gate with neat diagram and truth table. **10**

(ii) What are the benefits of digital communication? Explain the benefits with necessary diagrams. What are the disadvantages of digital communication? **10**

(iii) What is pulse modulation? Explain PAM, PWM and PPM. **10**

Q5. Attempt any **four:**---(5 marks each) **20**

(i) The intrinsic stand-off ratio for a UJT is determined to be 0.6. If the inter-base resistance is 10 KΩ, what are the values of R_{B1} and R_{B2} ?

(ii) Calculate the operating point for the fixed bias n-channel JFET circuit with V_{DD} = 12 V, R_D = 2KΩ, V_{GG} = -1.5 V, I_{DSS} = 6mA and V_P = -1.8V. (Given V_{GSQ} = - 0.5 V)

(iii) In differential amplifier with double ended input and single ended output circuit using discrete components has V_{CC} = 15 V, V_{EE} = -15 V, R_C = 33 KΩ and R_E = 47 KΩ. The left silicon transistor has β_{dc} = 100 and the right silicon transistor has β_{dc} = 120. If V_{BE} = 0.7 V for silicon transistor and $V_1 = V_2 = 0$ V. What are the dc base currents in each silicon transistor? Calculate the input offset current and the input bias current.

(iv) First order active low pass filter has C = 0.1μF and R= 1kΩ . Calculate cut-off frequency. If R_F is 1kΩ and R_i is 1kΩ, calculate pass band gain. What will be the gain at cut-off frequency?

(v) A pulse width modulator using IC 555 has $V_{CC} = 12\,V$, $R = 9.1k\Omega$ and $C = 0.01\mu F$. The clock has frequency of 2.5 kHz. If a modulating signal has peak value of 2V, what is the period of the output pulse? What are the minimum and maximum pulse widths?

(vi) Draw a neat circuit diagram LM317 three terminal voltage regulator to obtain adjustable supply. Design the regulated voltage source using LM 317 so that its output voltage Vo = 9V and the minimum current through it is (I_{min}) 5 mA. (Given V_{ref} = 1.25 V and V_{in} =15V)

(vii) Explain CMOS inverter with neat diagram.

(viii) Draw neat diagram of TTL NOR gate and write its truth table.
