[TE|VI| CBGS| ETRX | CO | 24|05|18
Sub:- Computer Orgunization

Q.P. Code: 36597

Duration: 3 Hours **Marks: 80**

N.B : (1) Question No.1 is compulsory.

(2) Attempt any three questions from remaining questions.

(3) Figures to the right indicate full marks.

Q1(a) Explain restoring division algorithm and draw its flowchart. 5

(b) Describe the concept of Nanoprogramming. 5

(c) Compare paging and segmentation. 5

(d) Draw the register structure of IA-32 family 5

Q2 (a)What is the necessity of replacement algorithm? Explain how pages are replaced between cache memory and main memory using replacement policies :

(i) LRU (ii) FIFO 10

(b)Explain the structure of serial and parallel ports. What are the methods to access it? 10

Q3 (a) Explain in detail any one hardwired technique of control unit design. 10

(b) Explain various DMA transfer modes with diagrams. 10

Q4 (a) Explain the advantages of pipelining. Explain various types of pipeline hazards and solutions to prevent them. 10

(b) Explain concept of cache memory with reference to principle of locality and Hit ratio Draw and explain different architectures of cache memory. 10

Q5 (a) What are different addressing modes of IA-32 family? Explain with examples. 10

(b) Explain single bus and multiple bus organization. 10

Q6 (a) Explain the Virtual Address to Physical address Translation for the following specifications Virtual Memory=128k and Main Memory=32k, page size = 1k. Illustrate Page Fault with the help of a example. 10

(b) Explain execution of a complete instruction with details. How are branch instructions executed? Use Single Bus organization. 10