TE | VI | CBGS | ETRX | 30 | 11 | 18

Q.P. Code: 36598

Duration: 3 Hours **Marks: 80**

N.B : (1) Question No.1 is compulsory.

(2) Attempt any three questions from remaining questions.

(3) Figures to the right indicate full marks.

Q1(a)Consider the following code

```
for(m=10;m>0;m--)
{
a[m]=a[m]+2
}
x=y+2;
x=x%2;
```

State the spatial locality and Temporal Locality in the code. 4

(b) State the advantages of Vertical Microinstructions over Horizontal Microinstructions. 4

(c) Consider the execution of a Program with 15000 instructions by a linear pipeline processor with a clock rate of 25 Mhz. Assume that the instruction pipeline is 5 stages one instruction is issued per clock cycle. The penalties due to branch instructions are ignored .

i) Calculate the speedup factor as compared with Non Pipelined processor.

ii) What is efficiency and throughput of this pipelined processor? 4

(d) Compare the RISC and CISC features 4

(e) Differentiate between Cache Look Aside Architecture and Cache Look through Architecture. 4

Q2 (a) Explain the Write Techniques in Cache Memory .Explain how Snoopy Controller Is used to implement Cache Coherency. 10

(b) Consider a 4-way set associative Cache Mapping with Cache Block Size=16 bytes Cache size=8k, Main Memory Size =64k. Design a cache structure and show how the Processor address is interpreted. 10

Q3 (a) Explain the Virtual Address to Physical address Translation for the following specifications Virtual Memory=128k and Main Memory=32k, page size = 1k .Illustrate Page Fault with the help of a example. 12

(b) Compare Paging and Segmentation 8

Q4 (a) Explain the various I/O Data transfer Techniques. 8

(b) Explain Microprogrammed Control Unit and compare its Control Memory with Nano-Programming. 12

Q5 (a) Explain the different addressing modes of IA-32 with suitable examples. 8

(b) Write microinstructions for the instruction MOV [R_0], R_3 . Explain the Hardwired control unit with reference to the above instruction. Design a Combinational circuit to generate the RUN control signal using suitable control signals. 12

Q6) Write short notes on

a) Memory Interleaving 6

b) Flynn's Classification 7

c) Page Replacement policies 7