Sem-VI (Electronics) (CBSGS) 7/12/16.

Computer Organization.

Q.P. Code : 591802

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question **No.1** is **compulsory**.
(2) Attempt **any Three** questions from remaining **questions**.
(3) **All** questions carry **equal marks**.
(4) **Figures** to the **right** indicate **full marks**.

1. (a) Calculate the effective memory access time for **20**
M1: 50 ns access time,
M2: 400 ns access time and hit ratio of M1 : 0.95
(b) Explain nano-programming and enumerate is advantages.
(c) Explain the principles of locality of reference used in cache memories.
(d) Show the address decoding for 128KB ROM (32 bit memory) using 32 bit addresses.

2. (a) Explain hardwired control unit with a neat diagram. Describe clearly the generation of control signals with examples. **10**
(b) A 32 bit processor has a 32 bit memory address. It has 8KB of cache memory. The computer follows 4-way set-associative mapping with each cache line size being 16 bytes. Show the memory address format and explain the process of lookup. (Draw neat diagrams). **10**

3. (a) Explain the register structure of the IA-32 family with neat diagrams. Describe the functions of each register in brief. **10**
(b) Explain the paging mechanism. State advantages of paging and the importance of the Translation Look aside Buffer (TLB) in paging. **10**

4. (a) Compare CISC and RISC design philosophies in detail (atleast five points of difference). **10**
(b) State the advantages of pipelining. Explain various types of pipeline hazards and their solutions. Give examples. **10**

5. (a) Explain the multi-bus data path organization with a neat diagram. **10**
(b) Write a control sequence and explain the steps for the following instruction **10**
ADD R2, [R1]

6. Write short notes on : **20**
(a) Cache coherency
(b) Storage devices
(c) Flynn's classification
