## 2/12/2015 TE Sem VI Elex- (BGS- CO

**QP Code: 6348** 

	(3 Hours)	[Total Marks: 80]
N.B. :	<ul><li>(1) Question No. 1 is compulsory.</li><li>(2) Attempt any three questions from remaining questions.</li></ul>	
- 3 -	<ul><li>(2) All questions carry equal marks.</li><li>(3) Figures to the right indicate full marks.</li></ul>	8
Q1.		
9 9 9	<ul> <li>a) What is parallel processing?</li> <li>b) Write short note on nanoprogramming.</li> <li>c) Compare RISC and CISC machines.</li> <li>d) What is effect of multiple data paths in design of processor.</li> </ul>	
Q2.		
200	<ul> <li>a) Explain Booth's Algorithm . Solve (+7) * (-5) using Booth's Algo</li> <li>b) Compare Hardwired control unit and Microprogrammed control unit</li> </ul>	rithm. it.
Q3.	a)Consider main memory size as three pages. Following page address by execution of a program	trace is generated
9	2 3 2 2 1 5 4 ·2 3 1 4 4 2	2 4
E a	Assume main memory is cleared initially. Find page hit ratio by 1)FIFO 2) LRU 3) LFU replacement policies.	
	b) Explain IA-32 architecture in detail.	
Q4.	<ul><li>a) Explain Cache memory and describe Cache mapping techniques.</li><li>b) What is bus arbitration? What are different methods to resolve bus a</li></ul>	arbitration.
Q5.		
13	a)Explain advantages of interrupt driven I/O over polling. Explain interaccess with one example.	rupt driven I/O
*	b) Draw and explain microprogrammed control unit for multiplier.	
Q6. W	Vrite short note on any four	19 520
	<ul> <li>a. Pipeline Hazards.</li> <li>b. Memory Hierarchy</li> <li>c. Restoring Division algorithm.</li> <li>d. 8085 addressing modes</li> <li>e. Arithmetic Instructions in IA-32 architecture.</li> </ul>	

MD-Con. 9484 -15.