Time: 3 Hrs **Marks: 80**

1) **Question No.1 is compulsory.**
2) **Attempt any three question out of remaining five questions.**
3) **Assume suitable data whenever necessary.**

1)

a) Represent $(78)_{10}$ and $(0.6125)_{10}$ in single precision floating point. 05
b) Explain basic structure of 4 stage Pipeline. 05
c) List Different I/O Access Methods. Explain any one detail. 05
d) Differentiate between SRAM and DRAM. 05

2)

a) Explain in detail organization of Cache Coherent – Non Uniform Memory Access. 10

b) What are the different types of pipeline Hazards. 10

3)

a) Explain Restoring Division algorithm and Perform (14) ÷ (6) using it. 10

b) What is necessity of replacement algorithm? Show how pages are replaced between cache and main memory using replacement policies: 10
i) LRU
ii) FIFO
iii) LFU

4)

Explain Set Associative Mapping. Draw and explain a two-way set-associative mapping for cache that has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte addressable. 20

5)

a) What is micro programmed control? Explain in details. Write microinstruction for MOV R_0,[R_1]. 10
b) Describe Flynn's Classification for parallel computer architecture. 10

6) Write Short Notes on

a) Superscalar Architectures. 10

b) Memory segmentation 10

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