(3 Hours) **[Total Marks: 80]**

Note: 1.Question 1 is compulsory.
2.Solve any three out of remaining .
3.Assume suitable data if necessary
4.Draw proper diagrams

Q.1. Solve any four.

(a) Compare Biploar,NMOS and CMOS technologies (min three points) . **[05]**

(b) Design a 2:1 MUX using transmission gates and discuss advantages of use of transmission gate logic. **[05]**

(c) Implement $Y=\overline{(A.B)+(C.D)}$ using Dynamic Logic. **[05]**

(d) Compare Ram and ROM. **[05]**

(e) Explain clock generation techniques. **[05]**

Q.2 (a) Sketch and explain the general shape of the Transfer characteristics of NMOS inverter.Compare different types of inverters. **[10]**

(b) Compare the full scaling model with constant voltage scaling model for MOSFETS. Demonstrate clearly the effects of scaling on the device density, speed of the circuit, power consumption and current density of the gates. **[10]**

Q.3 (a) Implement D flip-flop using Static CMOS. What are other design methods for it?

(b) Explain READ and WRITE operation of 6-T SRAM cell in detail. **[10]**

Q.4 (a) What is ESD protection? Explain with example. **[10]**

(b) Explain Carry Look Ahead adder and it's advantages. **[10]**

Q.5 (a) What are different clock distribution schemes? Explain concept of Global and Local clock. **[10]**

(b) What are various decoders used in memory structures? Explain any one in detail. **[10]**

Q.6. Write short notes on **(any three)** **[20]**

(a) NORA ,Zipper Logic design
(b) Flash Memory
(c) CMOS latch-up and its prevention
(d) Sense Amplifier