Sem VI / CBSGS / ETRX / BVLSI D / N.D - II.

T3226 / T0862 BASIC VLSI DESIGN

Q.P. Code :10652

[Time: 3 Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B:
1. Question No. 1 is **compulsory.**
2. **Attempt any three questions from remaining five questions.**
3. **Assume suitable data where required.**
4. **Figures** to the **right** indicate **full marks.**

Q.1 **(Solve any 4)**

a] Compare BJT & CMOS technology in VLSI design. **05**

b] Implement the following function using Static CMOS. **05**

$$Y = \overline{(A + B)(C + D)}$$

c] Implement half adder circuit using static CMOS. **05**

d] Implement 4*4. NAND based ROM array. **05**

e] Explain importance of Low power design. **05**

Q.2 a] What are the different MOSFET Models? Give importance of MOSFET capacitances related to MOSFET's performance. **10**

b] Explain transfer characteristics for CMOS Inverter showing different regions. What is the effect of variation in W/L ratio? **10**

Q.3 a] Draw 6T SRAM cell and explain it's read & write operation. **10**

b] Explain Scheme for multiplication of 110*100 **10**

Q.4 a] Explain various techniques of clock generation & clock distribution. **10**

b] Implement 4:1 multiplexer using NMOS pass transistor logic. **10**

Q.5 a] Draw D Flip Flop using CMOS and explain the working. **10**

b] Draw CLA (carry lookahead adder) carry chain using Static CMOS logic. **10**

Q.6 Write Short notes on. **20**

a] Interconnect Scaling

b]Latch up in CMOS

c] Decoder in Memory Structure.

d] ESD protection.
