Q.P. Code :25127

[Time: Three Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B:
1. Question.No.1 is compulsory.
2. Solve any three questions from remaining five questions.
3. Draw neat diagrams and assume suitable data wherever necessary. Justify you assumptions.

Q.1 Attempt **any four**: 20

a) Differentiate between sequential and combinational circuits.
b) Convert SR flip-flop into T flip-flop.
c) Explain Fan in, Fan out, Noise Margin, Propagation Delay, Power dissipation concepts of digital IC.
d) Implement 16:1 MUX using 8:1 MUX.
e) Explain stuck at '0' & stuck at '1' fault model.

Q.2 a) Write a VHDL code to design 2:4 decoders. 10

b) Design a implement full adder using IC 74138 (3:8 decoder) 10

Q.3 a) What are the different types of memories available in digital electronics? Explain with one application each. 10

b) Design circuit with optimum utilization of PAL to implement following function 10

$$F1(W,X,Y,Z) = \sum m\ (1,3,4,6,9,11,12,14)$$

$$F2(W,X,Y,Z) = \sum (1,3,4,6,9,11,12,14,15)$$

$$F3(W,X,Y,Z) = \sum m\ (2,3,8,9,12,13)$$

Q.4 a) Design Mealy type sequence detector to detect a serial i/p "**101**" 10

b) Design and explain Parallel In Serial Out Shift Register. 10

Q.5 a) Write short note on Boundary Scan. 05

b) Design 4 bit synchronous up counter using JK FF. 10

05

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c) Eliminate redundant states & draw reduced state diagram:

PS	NS		OP
	X=0	X=1	Y
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

Q.5 Write short note on: (**solve any three**) 20

a) XC 4000 FPGA architecture
b) 2 i/p TTL NAND gate
c) De-Morgan's Theorem
d) JK FF & D FF

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