SE|MTRX|Sem-III|CBSGS|SH-2018

11|12|2018

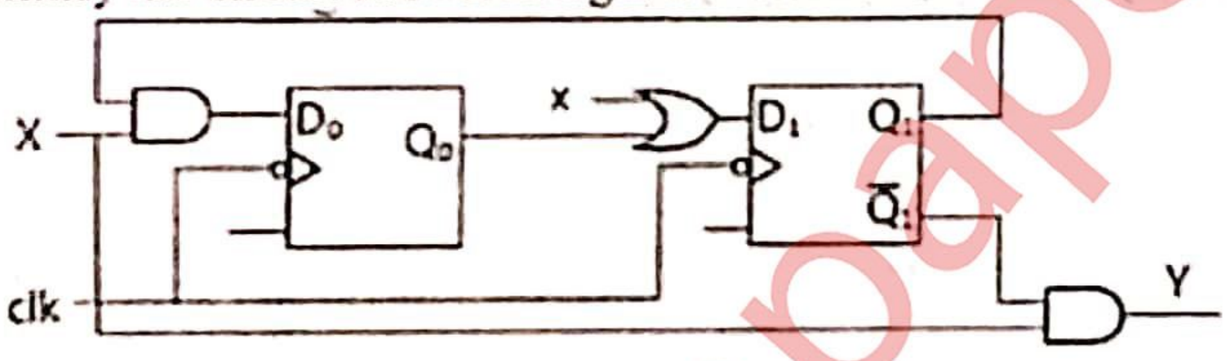
(3 hours) Total Marks: 80

N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three questions from remaining five questions.
(3) Draw neat diagrams and assume suitable data wherever necessary. Justify your assumptions.

1. (a) Write the disadvantages of a asynchronous counter. 5
(b) Draw truth table and logical diagram of a half subtractor. . 5
(c) Why NAND and NOR gates are called universal gates. 5
(d) Convert a T Flip Flop to D Flip Flop. 5

2. (a) Simplify the following using NAND gates only 5
$F1 = \Sigma m(1,2,4,7,10,12,13) + d(8,15)$
(b) Simplify the following using NOR gates only 5
$F = \Pi M(0,2,5,7,8,10,12,14)$
(c) Implement the following using 4:1 MUX and logic gates. 10
$P(A,B,C,D) = \sum m(1,2,6,7,10,12,13)$

3. (a) Identify the circuit shown in figure. Write the state table and state diagram for the same 10



(b) Eliminate redundant states and draw reduced state diagram. 10

Present state	Next state		Output	
A	B	C	1	0
B	F	D	0	0
C	D	E	1	1
D	F	E	0	1
E	A	D	0	0
F	B	C	1	0

4. (a) A combinational circuit is defined by the function 10
$F1(A,B,C) = \sum m(4,5,7)$
$F2(A,B,C) = \sum m(3,5,7)$
Implement this circuit with a PLA having 3 inputs,3 product terms and 2 outputs
(b) Write VHDL code for a 1 bit Full adder 10

5. (a) Draw truth table and circuit of JK FF using NAND gate. What is race around condition in JK FF and how is it avoided? 10
(b) Explain the basic characteristics parameters of digital logic families. 10

6. Write short note on **(any two)** 20
(a) Fault model
(b) Mealy and Moore machines
(c) Shift registers

****