SE MECA SEM-III (CBSGS) Sub:- D.E DT-16.K-16

QP Code : 726600

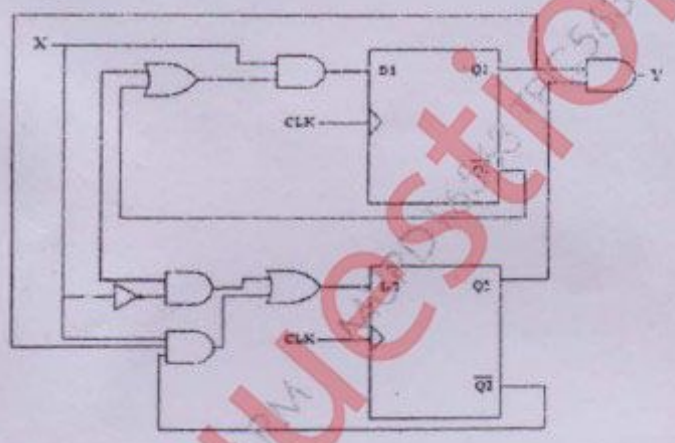
(3 Hours) **[Total Marks : 80**

N. B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **three** questions from remaining **five** questions.
(3) Draw neat diagrams and assume suitable data wherever necessary. Justify your assumptions.

1. (a) Convert a SR flip flop to JK flip flop. **5**
   (b) Define the term propagation delay and specify its value for a TTL gate and CMOS gate. **5**
   (c) Explain the glitch problem of a ripple counter with a waveform. **5**
   (d) Compare a PAL and PLA device. **5**

2. (a) Design a MOD 10 synchronous up counter using T flip flops. **10**
   (b) Write VHDL code for a I :8 Demultiplexer. **10**

3. (a) Design 8-bit BCD adder using 7483 and explain the operation with an example. **10**
   (b) Analyze the clocked synchronous machine shown below and write excitation equations, excitation table and state table. Draw the state diagram. Assume x = 0 and 1. **10**



4. (a) What is Multiplexer Tree? **10**
   Implement the following using 8:1 MUX using only NAND gates
   $P(A,B,C,D)= \sum m(0, 1, 2,4,5,7,10, 13,15) + d(3, 11)$
   (b) Design a circuit to implement the following functions with optimum utilization of PLA having 3 inputs, 3 product terms and 2 outputs. **10**
   $F1(A,B,C)= \sum m(4,5,7)$
   $F2(A,B,C)= \sum m(3,5,7)$

[TURN OVER

5. (a) Implement a sequence detector using Mealy machine to detect a sequence ... 11 0 1... using D flip flop and logic gates. **10**

(b) Find reduced SOP form and implement the same using only NAND gates: **10**

(i) $f(A,B,C,D)= \sum m(0,6,7,9,12,15)+\sum d(1,4,11)$

(ii) $f(W,X,Y,Z)= \pi M(0,1,2,8,9,10,12,13,15)$

6. Write short notes on (any **three**) **20**

(a) CMOS Inverter

(b) Fault Model

(c) Frequency division in asynchronous counters

(d) Shift Registers
