## Digital Electronics INST - CBGS /12-05-15 Sem-III QP Code: 30560 (3 Hours) [Total Marks: 80 N.B: (1) Question No. 1 is compulsory. (2) Attempt any THREE questions from remaining. (3) Figures to the right indicate full marks. (4) Assume suitable data if necessary. 1. Answer the following:-(a) State and prove De Morgan's theorems. (b) Implement 4:1 MUX using logic gates. (c) Explain the difference between combinational and sequential circuits. (d) Simplify the following expression using K Map. $F = \sum (0,2,5,7,8,10,13,15)$ 2. (a) Convert :-[10] i. (1010.101)<sub>2</sub> to Decimal. ii. (1085)<sub>10</sub> to Octal. iii.(1011)<sub>2</sub> to Gray. iv. $(34FB)_{16}$ to Binary. v. (177.1)8 to Binary. (b) Perform: -[05] i. Add $(9BDE)_{16}$ and $(ABCD)_{16}$ ii Divide 110110 by 101 (c) Compare demultiplexer and decoder. [05] 3. (a) Prove the following using Boolean algebra and draw the logic circuit. [10] $(A+B)(A+\overline{B}) = A$ i. $AB+\overline{A}C = AB+\overline{A}C+BC$ ii. (b) Convert JK flip-flop to T flip-flop and D flip-flop. [10]4. (a) Design 4 bit Binary to Gray code converter. T101 [10] (b) Implement full adder using logic gates. (a) Design a MOD 5 synchronous counter using JK flip flops. [10] (b) What is Shift register? Explain the working of 4 bit bidirectional shift register. [10] [20] 6. Write note on: - (any Four)

(a) PAL and PLA, (b) ALU, (c) Priority Encoder, (d) ECL Family,

(e) Basic dynamic RAM Cell.

FW-Con. 9414-16.