(Time: 3 Hours) **Marks: 80**

N.B. : (1) Question No. 1 is compulsory.
(2) Solve any three questions from the remaining five
(3) Figures to the right indicate full marks
(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 Attempt any 4 questions. [20]
(a) Explain bleeder resistor and critical inductance.
(b) Explain zero temperature drift biasing.
(c) Explain effect of bypass capacitor and coupling capacitors on frequency response of amplifier
(d) Draw and explain high frequency model of BJT for CE configuration.
(e) Draw and explain small signal model of FET.

Q.2 (a) Design single stage *RC* coupled CS amplifier using self-bias method to meet following specifications: $|Av|$ =18, *Vo*= 2.5 Vrms, I_{DSS} = 7 mA, g_{mo} = 5600 µS, *Vp*=2.5 V, r_d=50 kΩ. [15]
(b) Calculate *Av*, *Zi* and *Zo* for the circuit designed in Q.2(a). [05]

Q.3 (a) A full wave rectifier using a centre tapped transformer with two diodes gives output of 250 V and current is 100 +/- 25 mA. If the ripple factor is 0.001.Calculate the specification of the devices and components required if the filter used is *LC* filter. [12]
(b) Explain the basic fabrication steps of passive elements. [08]

Q.4 (a) What is biasing? What is the need of biasing? Derive the expression for stability factor of collector to base bias circuit. [10]
(b) Calculate *Q*-point (I_{CQ} & V_{CEQ}) and stability factor (*S*) for the circuit shown in Fig. 4(b). [10]

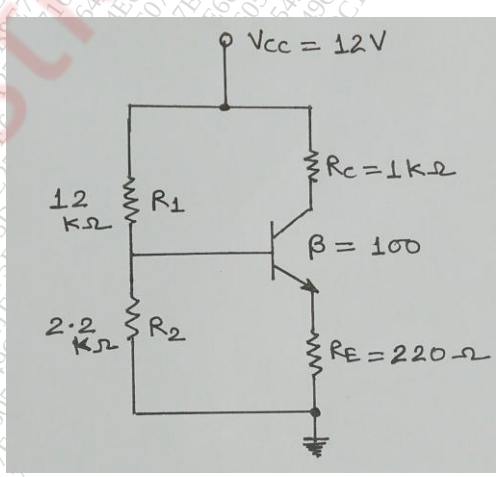

Fig. 4(b)

Q.5 (a) Derive the expressions for *Ai*, *Av*, *Zi*, *Zo* for CE amplifier with unbypassed R_E. [15]
(b) State and explain Miller's Theorem. [05]

Q.6 (a) Sketch the frequency response for the circuit shown Fig. 6(a) where C_1 = 0.5 μF, C_2 = 1 μF, C_S = 10 μF, C_{gs} = 5 pF, C_{gd} = 2 pF, C_{ds} = 3 pF. Take I_D = 3 mA. [15]

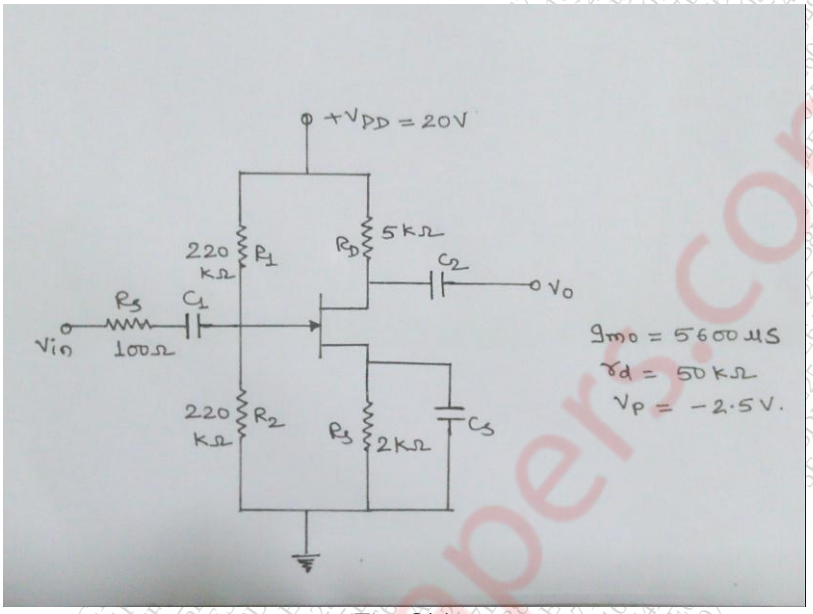

Fig. 6(a)

(b) Write a short note on small signal model of diode. [05]

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