	(3 Hours)	80 Marks
N.B.:	(1) Question No. 1 is compulsory.	//
	(2) Solve any three questions from the remaining five	1
	(3) Figures to the right indicate full marks	
	(4) Assume suitable data if necessary and mention the same in answer s	heet.
Q.1	<ul> <li>a) If F(A, B, C) = ∑m(0,3,5,7) with its truth table and express F in SOP and POS form</li> <li>b) Compare TTL and CMOS Logic families</li> <li>c) Perform the following operation using 2's compliment <ul> <li>i) (7)<sub>10</sub> - (15)<sub>10</sub></li> <li>ii) (50)<sub>10</sub> - (2A)<sub>16</sub></li> </ul> </li> </ul>	[20]
	Comment on results of (i) and (ii) d) Compare SRAM with DRAM	
Q.2	a) Implement following Boolean function using 8:1 multiplexer $F(A, B, C, D) = \overline{A} B \overline{D} + A C D + \overline{B} C D + \overline{A} \overline{C} D$	[10]
	b) Design 3 bit Binary to Gray code Converter	[10]
Q.3	a) What are shift registers? How are they classified? Explain working of a one type of shift register.	
	b) Write VHDL code for 3 bit up counter.	[10]
Q.4	<ul> <li>a) Explain Master slave JK Flip flop</li> <li>b). Convert T flip flop to D flip flop.</li> <li>c) Minimize the following expression using Quine McClusky Technique F(A, B, C, D) = ∑m(1,3,7,9,10,11,13,15)</li> </ul>	[5] [5] [10]
Q.5	<ul> <li>a) State and prove Demorgan's theorem</li> <li>b) b) Convert (532.125)<sub>8</sub> into decimal, binary and hexadecimal.</li> <li>c) Explain Full Adder circuit using PLA having three inputs, 8 product ter and two outputs.</li> </ul>	[5] [5] ms [10]
Q.6	a) Prove that NAND and NOR gates are universal gates	[10]
	b) Draw and explain 3 bit asynchronous binary counter using positive ed triggered JK flip flop. Draw the waveforms.	dge [10]

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