Time: 3 Hours **Max Marks: 80**

N:B: 1. Question No. 1 is compulsory.
2. Out of remaining questions, attempt any three questions.
3. Assume suitable additional data if required.
4. Figures in brackets on the right hand side indicate full marks.

Q.1 (A) The Gray code for decimal number 6 is equivalent to **(01)**
i) 0100 ii) 0001
iii) 0101 iv) 0110
Prove it. **(04)**

(B) Which of the following is correct statement: **(01)**
i) PLA contains a fixed AND array and a programmable OR array.
ii) PLA contains a programmable AND array and a programmable OR array.
iii) PAL contains a fixed AND array and a programmable OR array.
iv) PAL contains a programmable AND array and a programmable OR array.
Draw the structure of correct statement. **(04)**

(C) Which of the following expression is equivalent to $Z = A\,\overline{B} + C$ where A represents MSB and C represents LSB of the binary numbers? **(01)**
i) $Z = \sum m(0, 2, 6)$. ii) $Z = \Pi M(1, 3, 4, 5, 7)$.
iii) $Z = \sum m(1, 3, 4, 5, 7) + d(6)$. iv) $Z = \Pi M(0, 2, 6)$.
Prove it. **(04)**

(D) A single 4-bit magnitude comparator IC 7485 can compare maximum **(01)**
i) two 4-bit numbers ii) two 5-bit numbers
iii) two 8-bit numbers iv) two 10-bit numbers
Draw its corresponding diagram **(04)**

Q.2 (A) Implement the following Boolean equation using single 4:1 MUX and few logic gates: $F(A, B, C, D) = \sum m(0, 2, 5, 6, 7, 9, 12, 15)$. **(10)**

(B) Write the VHDL code for Fibonacci Series Generator sequential circuit. **(10)**

Q.3 (A) Design synchronous counter using D type flip flops for getting the following sequence: $0 \rightarrow 2 \rightarrow 4 \rightarrow 6 \rightarrow 0$. **(10)**
Take care of lockout condition.

(B) Compare SRAM with DRAM. **(05)**

(C) What are the Universal Gates? Why are they so called? Design any one Basic Logic Gate using only Universal Gates. **(05)**

Q.4 (A) Draw a neat circuit of BCD adder using IC 7483 and explain. **(10)**

(B) Using Quine Mc'Clusky method, minimize the following: **(10)**
$F(A, B, C, D) = \sum m(0, 3, 5, 7, 8, 11, 13, 15)$.

Q.5 (A) With neat diagram, explain the working of Universal Shift Registers. Give its applications. **(10)**

(B) Analyze the circuit given in Figure 5(B). Assume initial state as A=0, B=0. Complete a state table that shows the behavior of this state machine. Is this a Moore or Mealy machine? (Explain with a sentence) **(10)**

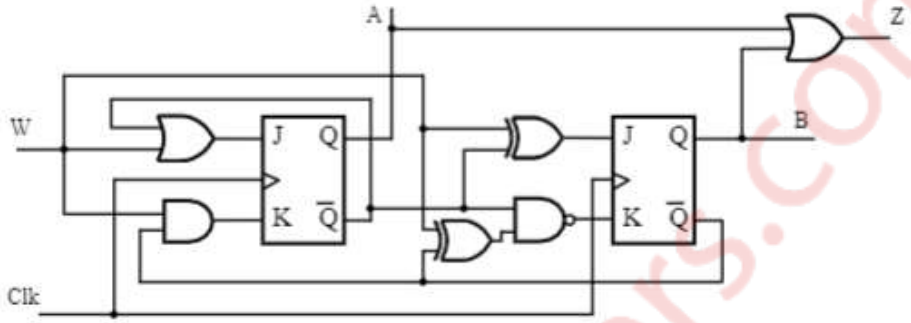

Fig. 5(B)

6. (A) Convert T type flip flop into D type flip flop. **(05)**

(B) Compare Moore with Mealy circuits. **(05)**

(C) Compare PAL with PLA. **(05)**

(D) Compare FPGA with CPLD. **(05)**

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