[Time: 3 Hours] **[Total Marks : 80]**

N.B: 1) Question no. 1 is compulsory.
2) Attempt any three out of the remaining five questions
3) Use suitable data, wherever necessary.

Q1. Solve any four : - 20

A) Compare Moore & Mealy models.

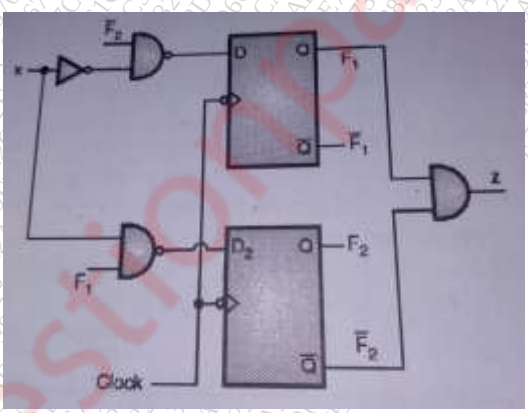
B) State various types of boxes used for drawing the ASM chart.

C) Give classification of RTL operations.

D) Define Clock skew and Metastability.

E) Compose VHDL code for implementation of D Flip Flop.

Q2. A) Analyze the sequential machine shown in figure and obtain the state diagram for the same. 10



B) Draw the data unit for the following RTL description. 10

MODULE : DATA MOVER

MEMORY : A[2]; B[2]; C[2]

INPUT : X[2]

OUTPUT : Z[2]

1. A←X 2. C←A 3. B←C[0], C[1] 4. C← A v B 5. Z=C.

END SEQUENCE.

Q3. A) Shown below is the state table for sequential Machine ,using implication chart method, eliminate redundant and obtain minimized state diagram. 10

Present state	Next State		Output Z	
	X=0	X=1	X=0	X=1
S_0	S_4	S_3	0	1
S_1	S_5	S_3	0	0
S_2	S_4	S_1	0	1
S_3	S_5	S_1	0	0
S_4	S_2	S_5	0	1
S_5	S_1	S_2	0	0

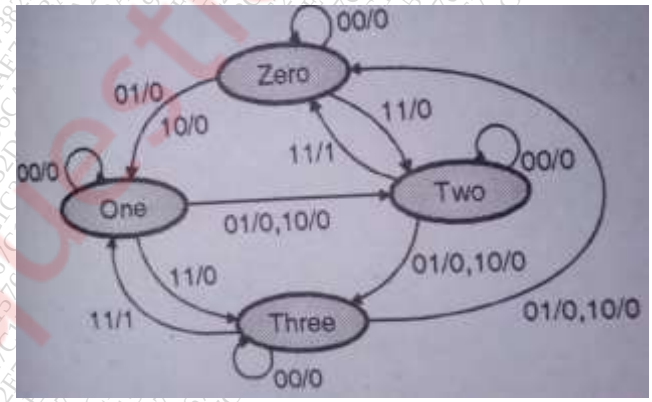
B) Design a sequential circuit using Mealy Machine to detect an overlapping sequence as follows.....1010..... 10

Q4. A) Design MOD 11 synchronous counter usind T Flip Flop . 10

B) Write VHDL code for full adder usind half adder as a component. 10

Q5. A) Draw with logic diagram , a simple 8X4 diode ROM. 10

B) Write a VHDL code for the state diagram shown make use of process statement.



Q6. Write Short Notes on. 20

(i) PLA
(ii) Xilinx XC 9500 CPLD .
(iii) Field programmable gate array (FPGA).
(iv) Various modelling styles in VHDL.
