[Time: 3 Hours] **[Marks:80]**

N.B: 1) Question no. 1 is compulsory.

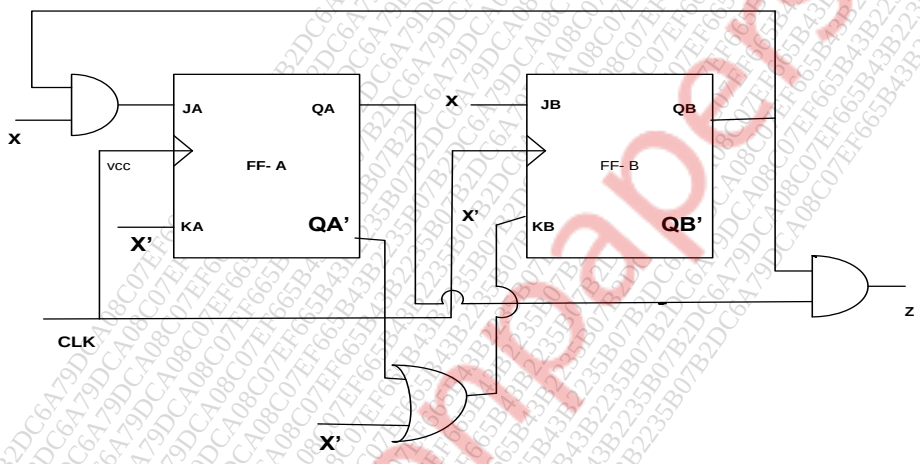
2) Attempt any three out of the remaining five questions

3) Use suitable data, wherever necessary.

Question 1: Attempt **any four** questions from the following. (20)

I. I) Differentiate between Mealy Machine and Moore Machine
II. Draw the Standard symbols for ASM Charts.
III. Compose VHDL code for Implementation of D Flip Flop
IV. Differentiate between signal and Variable.
V. Differentiate between IC 7490, IC 7492, IC 7493

Question 2 (A) Analyse the sequential circuit shown below. Derive the excitation equation, Transition table and state diagram. (10)



Question 2 b) Draw the data unit for the following RTL description (10)

Module; Data Mover
Memory: A [2]; B [2]; C [2].
Inputs: X [2].
Outputs: Z [2].

1. A ← X.
2. C ←$\bar{A}$.
3. B ← X [1], X [0].
4. C ← A V B.
5. Z = C.

End sequence.

Question 3(A) Shown below is the state table for sequential machine, using implication chart method, eliminate redundant states and obtain minimized state diagram. (10)

X1X2	00	Z	01	Z	10	Z	11	Z
A	D	0	D	0	F	0	A	0
B	C	1	D	0	E	1	F	0
C	C	1	D	0	E	1	A	0
D	D	0	B	0	A	0	F	0
E	C	1	F	0	E	1	A	0
F	D	0	D	0	A	0	F	0
G	G	0	G	0	A	0	A	0
H	B	1	D	0	E	1	A	0

Question 3(B): Construct ASM chart of sequence detector which detects the sequence 1001. The output Z becomes 1 along with the last correct bit of the sequence. (10)

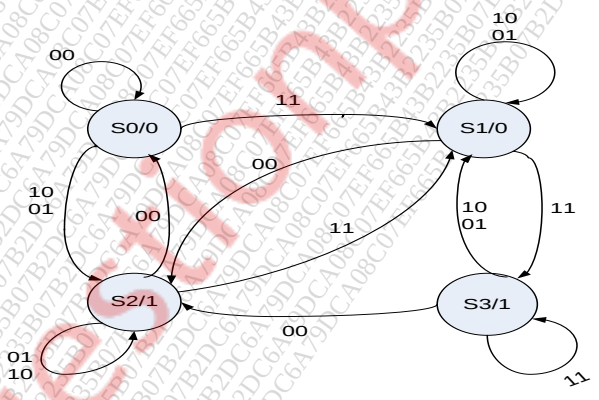
Question 4(A): Create VHDL code for Implementation of 4:1Multiplexer using two different architecture modelling styles.

Question 4(B): Design a MOD 61 up counter using IC 74163 and explain its working. (10)

Question 5(A): Design full subtractror using PLA. (10)

Question 5(B): Explain input-output block architecture for FPGA 4000 family. (10)

Question 6 (A): Write VHDL code for the state diagram given below. (10)



Qustion 6(b): Evaluate the value of output variable for following signal declarations. (10)

```
SIGNAL a: BIT: = '1';
SIGNAL b: BIT_VECTOR (3 DOWNTO 0):= "1100";
SIGNAL c: BIT_VECTOR (3 DOWNTO 0):= "0010";
X1 <= c & b;      ------  X1< =_________
X2 <= b XOR c;   -------  X2< =_________
X3 <= b sll 2;       ------  X3< =_________
X4 <= b rol 3;      ------  X4< =_________
X5 <= a AND NOT b (0) AND NOT c(1); ----X5<=_________
```

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