(3 Hours)   **[Total Marks: 80]**

N.B: 1) Question no. 1 is compulsory.
       2) Attempt any three out of the remaining five questions
   3) Use suitable data, wherever necessary.

Question 1 : Attempt **any four** questions from the following.   20

  i.   Explain Inspection Method of State Reduction.
  ii.   Draw the Standard symbols for ASM Charts.
  iii. Write short note on VHDL Features.
  iv.   Compose VHDL code for Half Adder using Behavioural Modelling Style.
  v.   Design & Explain a MOD-10 counter with counting sequence 0,1,2,...9,1,2,3,...using IC
        74x163

Question 2: Analyse the sequential state machine shown below. Obtain the excitation
equation, transition table and state diagram for the same.   10
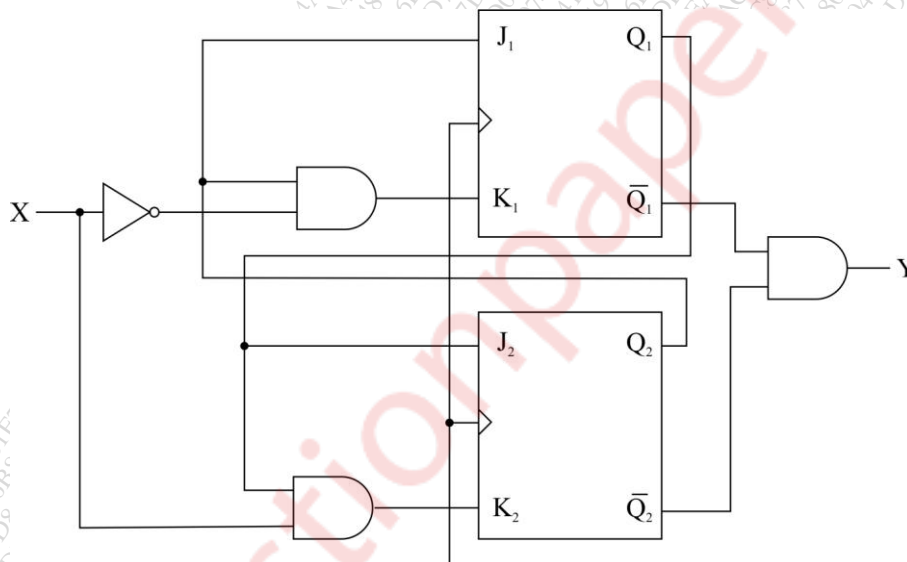
Question 2 b)With diagrams explain the meaning of following RTL statements (Assume all registers
are 2-bit)   10
    1. $Y \leftarrow X$
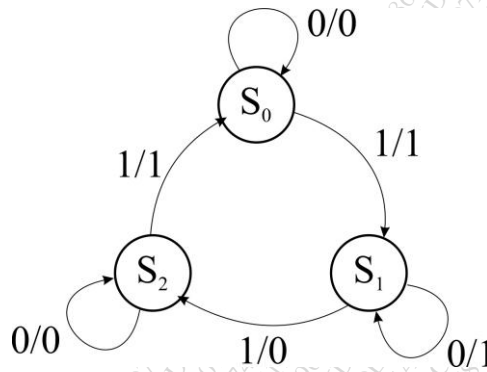   2. $C \leftarrow A \vee B$
    3. $(\overline{X[1]}, X[1]/(5,7))$.

Question 3 a) Reduce the state of the following state table using Partition Method.   10

Present State (PS)	Next State (NS), Output (Z)	
	X=0	X=1
A	C,0	F,0
B	D,1	F,0
C	E,0	B,0

81614   **Page 1 of 2**

6B81E74A486D7D074196DEAC87804DD8

D	B,1	E,0
E	D,0	B,0
F	D,1	B,0

Question 3 b) Draw the Standard symbols for ASM Charts and convert the following state diagram to ASM Chart. 10

Question 4 a) Draw block diagram of 8:3 Octal to Binary Encoder and Compose VHDL code for same using behavioural modelling style. 10

Question 4 b) Design following using IC 7490: 10

1. MOD 97 Counter 2. MOD 45 Counter

Question 5 a) Discuss CPLD Xilinx XC 9500 architecture with neat block diagram. Describe main features. 10

Question 5 b) Design Full Adder using PLA. 10

Question 6 a) Explain in detail Structure of VHDL Module and also explain port modes in VHDL.

10

Question 6 b) Explain the application of shift register. 10

_____