Paper / Subject Code: 38903 / COMPUTER ORGANIZATIN AND ARCHIECTURE

S.E.SEM IV / COMP / CREDIT BASE / MAY 2019 / 17.05.2019

Q.P. Code: 40879

(80 Marks)

• Question no. 1 is compulsory.

- Answer any three questions from question no. 2 6.
- Assume suitable data, if necessary.



(3 Hours)

Q.1.	Answer	following	questions	in	brief.
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	а	Convert the following number 256.325 into IEEE 32 bit Single Precision Format and IEEE 64 bit Double Precision Format	(05)
	b	Discuss difference between RISC and CISC processors.	(05)
	С	Explain function of 8089 I/O processor in brief.	(05)
	d	Differentiate between SRAM and DRAM	(05)
	u	Differentiate between Skalvi and Dkalvi	(03)
Q.2.	a.	Explain cache consistency and coherency with suitable examples. Also, give methods to maintain cache consistency.	(10)
	b.	Explain DMA based data transfer techniques.	(10)
	D.	Explain Divia based data transfer techniques.	(10)
Q.3.	a.	Explain how Virtual Address is translated to Physical address with suitable	(10)
	L.	example.	(40)
	b.	Compare between Cache Look Aside Architecture and Cache Look through	(10)
		Architecture	(00)
Q.4.	a.	Explain the Bus Arbitration Techniques	(80)
	b.	Explain hardwired Control Unit with help of neat diagram. Compare it with microprogrammed control unit.	(12)
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Q.5.	a.	What is TLB? Explain working of TLB.	(10)
	b.	Describe register organization within CPU.	(10)
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Q.6.	-VV I	rite short note on	
29.0	a.	Hazards in Pipelining	(05)
9-270	b.	Interrupt driven I/O	(05)
\$ 8°	See the	Interleaved memory	(05)
150 C	2 2 10	Modes of DMA	(05)
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