SE - Sem - IV (Biomed.)
Logic Circuits

10/6/14.

QP Code : NP-19842

(3 Hours) (22) **[Total Marks : 80**

N. B. : (1) Attempt any **four** questions from **six** questions.
(2) Figures to the **right** indicate **full** marks.

1. Answer the following questions :– **20**
   (a) Convert J-K Flip Flop to T FlipFlop
   (b) Design a half subtractor with only NAND gates
   (c) Why is Excess-3 called a self-complementing code
   (d) What do you understand by positionally weighted codes
   (e) State and prove 'DeMorgan's Theorem'.

2. (a) Design the following gates :– **8**
   (i) NOR using NAND
   (ii) NAND using NOR
   (b) Design Gray ($G_3G_2G_1G_0$) to Binary ($B_3B_2B_1B_0$) converter **12**

3. (a) Explain the following :– **8**
   (i) Standard and non-standard sop forms
   (ii) Standard and non-standard pos forms
   (b) Design a 2 bit multiplier (A_1A_0 with B_1B_0) **8**
   (c) Explain hazards in combinational circuits. **4**

4. (a) Design 32 : 1 Multiplexer using two 16 : 1 multiplexers. **5**
   (b) Draw and explain 2 input TTL NAND gate. What are salient features of TTL family. **10**
   (c) Explain bidirectional shift register **5**

5. (a) Design synchronous mod 4 up-down counter using JK Flipflop **10**
   (b) Explain the operation of S-R FlipFlop using NAND gates. What is a race around condition. **10**

6. Write short notes on :– **20**
   (1) Hamming code
   (2) Quine McClusky's technique
   (3) Counter ICS
   (4) Shaft position encoding.

Con. 13347-14.