4-Dec-2019 1T01118 - B.E.(ELECTRONICS)(SEM VIII) (CBSGS) / 53001 - CMOS VLSI Design

66577

Max Marks: 80

Time: 3 Hours

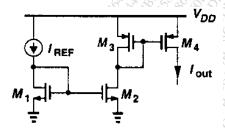
1) Question No.1 is compulsory

- 2) Solve any three questions from the remaining questions.
- 3) Assume suitable data if necessary.

1 Solve any four

N.B.

- (a) For an NMOS device operating in saturation, plot W/L versus V_{GS}-V_{TH} if
 a. I_D is constant
 b. gm is constant
- (b) Find the drain current of M4 if all transistors are in saturation



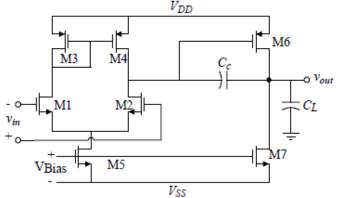
- (c) Compare full custom and semi-custom design in terms of its trade-offs and applications 5
- (d) Explain Non-ideal effects in PLL. 5
- (e) Compare various op amp topologies 5
- 2 (a) Compare common source amplifier with following loads 10
 - a) NMOS diode connected load
 - b) PMOS diode connected load
 - c) Current source load
 - d) Triode load

 $V_{b} \longrightarrow V_{aut}$

- a. Redraw the above circuit using thermal noise current source
- b. Write the expression for total output thermal noise voltage
- c. Write the expression for output thermal noise voltage referred to the gate of M1
- d. Why should gm₁ be maximized and gm₂ be minimized in the above circuit.

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3 Design two stage operational amplifiers that meet the following specifications



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Av > 3000V/V $V_{DD} = 2.5V$ $V_{SS} = -2.5V$

Gain Bandwidth = 5MHz, Slew Rate $> 10V/\mu s$, 60° phase margin,

 $0.5V < V_{out}$ range < 2V,

ICMR = -1.25V to 2V,

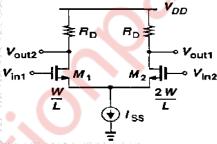
 $P_{diss} \le 2 \text{ mW}, C_L=10 pF$

Use $K_N = 100 \mu A/V^2$, $K_P = 20 \mu A/V^2$, $V_{TN} = |V_{TP}| = 0.5 V$, $\lambda_N = 0.06 V^{-1}$,

 $\lambda_P = 0.08V^{-1}$, Cox=2.47fF/ μ m².

Verify that the designed circuit meets required voltage gain and power dissipation specifications

4 (a) Analyze following circuit to get voltage gain equation if M₂ is twice wide as that of 10 M₁ and Vin₁=Vin₂



- (b) Derive the expression Voltage gain Av and Output impedance Ro for Source 10 follower circuit
- 5 (a) Derive equation of differential gain, common mode gain and CMRR of a differential amplifier circuit.
 - (b) Explain the switched capacitor amplifiers in detail with appropriate diagrams
- 6 Write short notes on (any four)
 - (a) Charge pump PLL 5
 - (b) Stability and frequency compensation of two stage Opamp 5
 - (c) Band Gap references(d) Performance parameter of VCO5
 - (e) AMS Design flow 5

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